

Appl. No. 10/710,175
Amdt. dated February 07, 2006
Reply to Office action of December 19, 2005

Amendments to the Claims

Listing of Claims:

Claims 1-13 (cancelled)

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Claim 14 (previously presented) : An apparatus for adjusting a phase difference between two input signals, the apparatus comprising:

- a first buffer for buffering a first input signal and outputting a first output signal;
- 10 a first DAC for outputting a first control voltage corresponding to a first digital value representative of a phase delay;
- a first variable capacitor coupled to the first DAC and the first buffer, the capacitance value of the first variable capacitor corresponding to the first control voltage;
- 15 a second buffer for buffering a second input signal and outputting a second output signal;
- a second DAC for outputting a second control voltage corresponding to a second digital value representative of a phase delay; and
- a second variable capacitor coupled to the second DAC and the second buffer,
- 20 the capacitance value of the second variable capacitor corresponding to the second control voltage;
- wherein by controlling at least one of the first and the second digital values, the phase difference between the first input signal and the second input signal are adjusted.

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Claim 15 (previously presented) : The apparatus of claim 14 being implemented in a receiver.

Appl. No. 10/710,175
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Claim 16 (previously presented): The apparatus of claim 14 being implemented in a transmitter.

5 Claim 17 (previously presented): The apparatus of claim 14 being implemented in a transceiver.

Claim 18 (previously presented) : The apparatus of claim 14, wherein the first input signal and the second input signal are differential signals.

10 Claim 19 (previously presented) : The apparatus of claim 14, wherein the first input signal and the second input signal are an in-phase signal and a quadrature-phase signal respectively.

15 Claim 20 (previously presented) : The apparatus of claim 14, wherein the first input signal and the second input signals are clock signals.

Claim 21 (previously presented) : The apparatus of claim 14, wherein the first input signal and the second input signal are RF signals.

20 Claim 22 (previously presented) : The apparatus of claim 14, wherein the first variable capacitor and the second variable capacitor are voltage-controlled capacitors.

25 Claim 23 (previously presented) : The apparatus of claim 22, wherein the voltage-controlled capacitors are MOS-based voltage-controlled capacitors.

Claim 24 (previously presented) : The apparatus of claim 22, wherein the

Appl. No. 10/710,175
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voltage-controlled capacitors are P+/N well junction voltage-controlled capacitors.

- Claim 25 (previously presented) : A method for adjusting a phase difference between
- 5 two input signals, the method comprising:
- buffering a first input signal and outputting a first output signal;
- buffering a second input signal and outputting a second output signal;
- providing at least one of a first digital value and a second digital value
- representative of a first phase delay and a second phase delay respectively;
- 10 and
- adjusting a capacitance value of a first variable capacitor with a first control
- voltage generated from the first digital value or adjusting a capacitance
- value of a second variable capacitor with a second control voltage
- generated from the second digital value, to adjust the phase difference
- 15 between the input signal and the output signal.

Claim 26 (previously presented) : The method of claim 25, wherein the first input

signal and the second input signal are differential signals.

- 20 Claim 27 (previously presented) : The method of claim 25, wherein the first input
- signal and the second input signal are an in-phase signal and a quadrature-phase
- signal respectively.

- Claim 28 (previously presented) : The method of claim 25, wherein the first input
- 25 signal and the second input signals are clock signals.

Claim 29 (previously presented) : The method of claim 25, wherein the first input

Appl. No. 10/710,175
Amdt. dated February 07, 2006
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signal and the second input signal are RF signals.

Claim 30 (previously presented) : The method of claim 25, wherein the first variable capacitor and the second variable capacitor are voltage-controlled capacitors.

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Claim 31 (previously presented) : The method of claim 30, wherein the voltage-controlled capacitors are MOS-based voltage-controlled capacitors.

Claim 32 (previously presented) : The method of claim 30, wherein the voltage-controlled capacitors are P+/N well junction voltage-controlled capacitors.

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